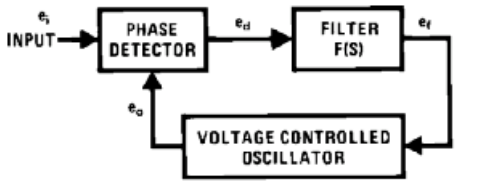
Communications Electronics Laboratory

Practical Session 2: PLL

2.1 Introduction

This practical session is based on the NE565 chip, a monolithic PLL (*Phase-Locked-Loop*) with working range reaching 500 KHz. The simplified block diagram for a PLL can be seen in figure 1.



TL/H/7:

FIGURE 1. Basic Phase Locked Loop

2.2 NE 565 integrated circuit

The NE565 chip is a general-purpose PLL. Figure 2 shows its block and pin diagrams.

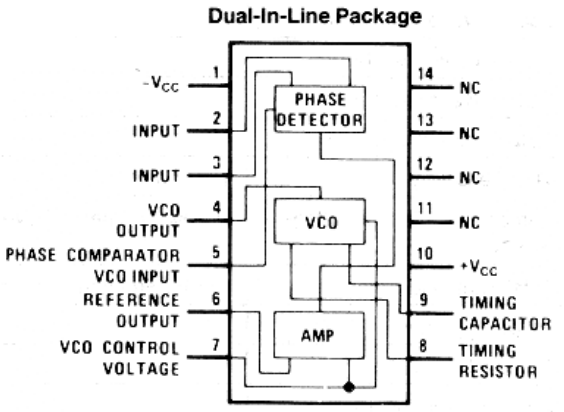


FIGURE 2. PLL NE565 block and pin diagrams.

VCO

The VCO free-running frequency is $f_0 \approx \frac{0.3}{R_0 C_0}$, where R_0 is the external resistor connected between pins 8 and +Vcc (10) and C_0 is the external capacitor connected between pin 9 and the ground.

Phase detector

The parameter that characterizes the phase detector is its sensitivity K_D (V/rad). It can not be altered by the user (internal parameter). In the NE565 datasheet $K_D = 0.68$ (V/rad) is given as a typical value for the sensitivity.

Loop filter

The gain in closed loop is determined by the expression $K_0 \times K_D$ (s^{-1}), where K_0 ((rad/s)/V) is the sensitivity of the VCO. In the NE565 chip the approximation $K_0 K_D \approx \frac{33.6 f_0}{V_C}$ (s^{-1}) is valid, where V_C is the circuit supply power.

The phase detector output is obtained in pin 7. Between pins 7 and 10, the NE565 has an internal resistance (R_1 = 3.6 kΩ) that can be used to build the loop filter. In most of the applications it is enough to connect one capacitor to pin 7. This capacitor in parallel with resistance R_1 produces a first order filter as shown in figure 3.

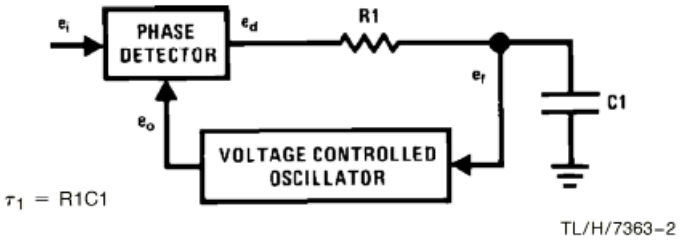


FIGURE 3. Loop filter.

In this case the transfer function of the loop filter is:

$$L(s) = \frac{1}{1 + sR_1C_1} = \frac{1}{1 + s\tau_1}$$

This transfer function for an ideal behaviour of the phase detector would be given by the expression:

$$\frac{\Phi(s)}{\Theta(s)} = \frac{L(s)}{L(s) + s}$$

When L(s) is a first order function the global response of the loop is given by the second order expression:

$$\frac{\Phi(s)}{\Theta(s)} = \frac{K}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where ζ is the damping factor and ω_n is the natural frequency of the system. The transfer function of the loop filter becomes:

$$\frac{\Phi(s)}{\Theta(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{K_0 K_D / \tau_1}{s^2 + s/\tau_1 + K_0 K_D / \tau_1},$$

The frequency response of the filter is shown in figure 4.

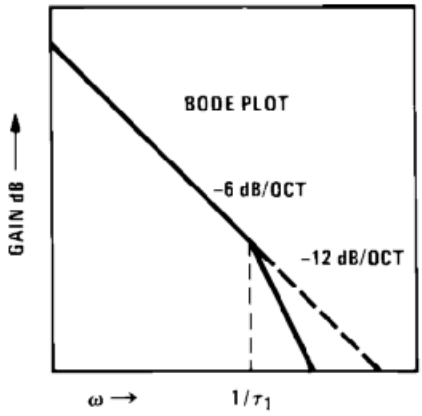


FIGURE 4. Closed loop transfer function.

- Lock range

The lock range is given by the range of input frequencies f_i to which the PLL can lock. This limit is determined by the phase detector if we consider that the VCO does not saturate. Suppose that the difference between the VCO output frequency f_o and the input frequency f_i is Δf. In order to lock to the input frequency, the VCO control voltage should be varied in $V_0 = \Delta f / K_0$ volts. If the loop amplifier has no gain, the VCO control voltage is directly given by the output voltage of the phase detector $V_D = K_D \theta_e$. Since the maximum phase shift that can be followed by the PLL is $|\theta_e| \le \pi/2$, we get the following expression for the lock range:

$$\Delta f_H = \pi K_0 K_D \approx \frac{16 f_0}{V_C}.$$

2.3 Practical session guidelines

PLLs can be used for coherent demodulation of amplitude modulated signals. The coherent demodulator block diagram is shown in figure 5.

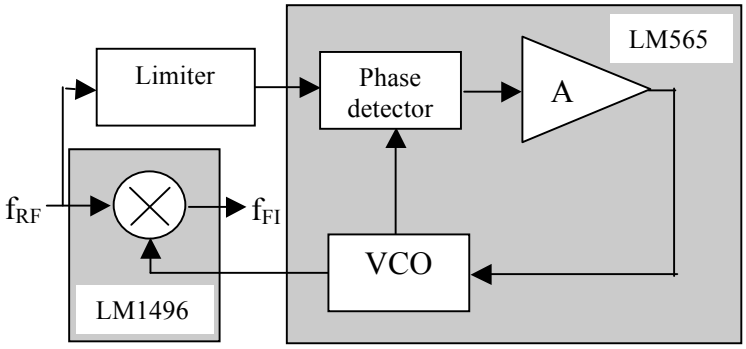


FIGURE 5. Coherent demodulator.

As shown in the figure above the MC1496 balanced modulator can be used together with the NE565 in order to accomplish the coherent demodulation.

- Modulate a 10 Khz carrier with a 1 Khz tone. Design and analyze the AM coherent demodulator following the scheme shown in figure 6.

  - Select properly components R_0 and C_0 so that the free-running frequency is 10 KHz using a 15V supply voltage.

  - You can replace the 2N3565 transistor by a 2N2222.

  - The capacitor values are given in μF.

  - The following table shows the correspondence between LM1596 and LM1496 pins.

LM1596	LM1496
1	1
2	2
3	3
4	4
5	5
6	6
7	8
8	10
9	12
10	14

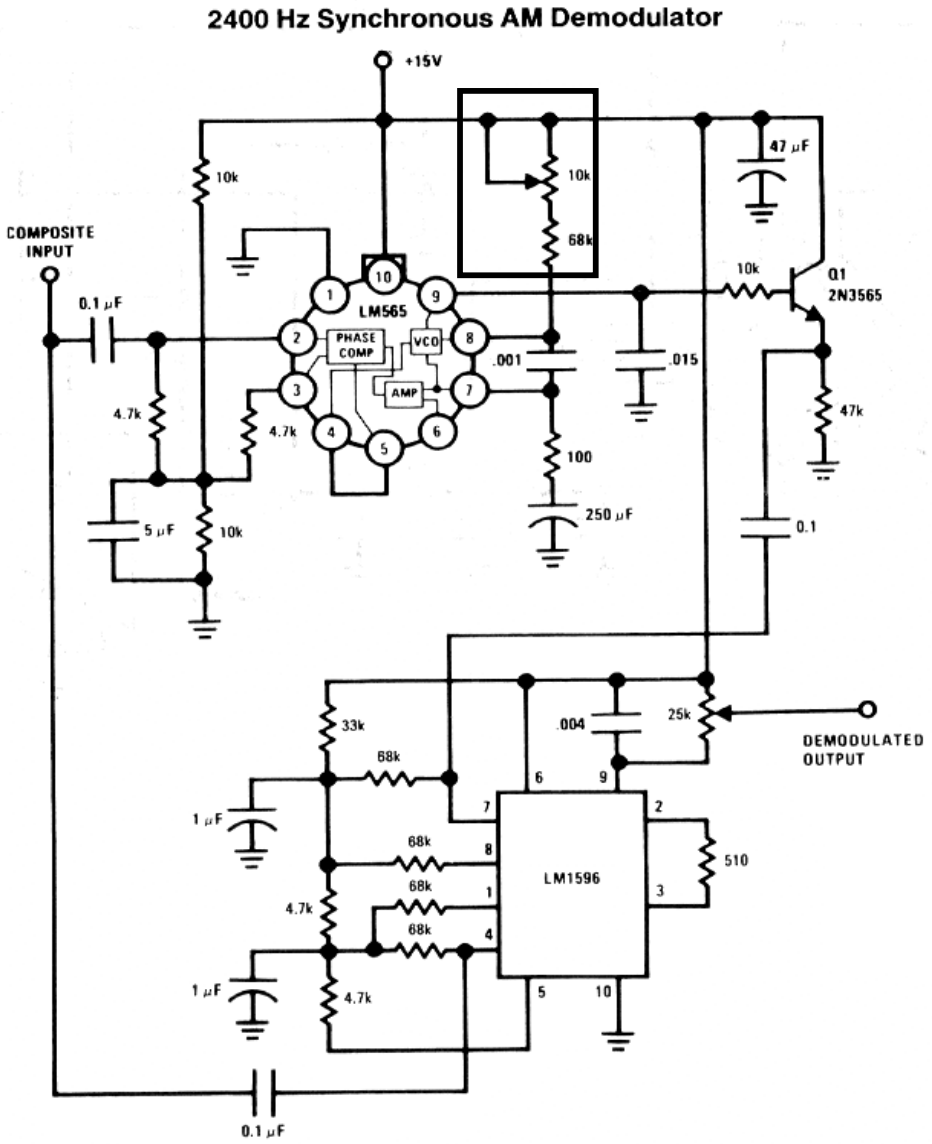


FIGURE 6. Coherent demodulator.

2.3.1 PLL characterization

Notice: in order to avoid the load of the mixer by the PLL disconnect the 0.1uF capacitor which connects the Q1 transistor emitter with pin 7 of the mixer LM1496/LM1596.

2.3.1.1 PLL free-running frequency measurement

With the input connected to ground measure the free-running frequency of the PLL in the Q1 transistor emitter.

2.3.1.2 Lock and track range measurement for different supply voltages

Measure the lock and track ranges of the PLL by introducing a sinusoidal signal in the circuit input and observing the output in the Q1 transistor emitter. Vary the supply voltage between 10 and 24 volts (in 2 volts steps). The report should contain the obtained curve.

2.3.2 Mixer characterization

2.3.2.1 LO rejection in IF.

With the circuit general input connected to 0 volts introduce a 1 V_{rms} and 10 KHz signal into the mixer through the 0.1μF capacitor which was disconnected in the previous step. Observe the output in order to verify the power level of the 10 KHz signal in pin 12 of the LM1496. Determine the LO rejection level in IF.

2.3.2.2 LO rejection in RF

Using the same scheme as in the previous step, measure the 10 KHz signal level in pin 4 of the LM1496. Determine the LO rejection level in RF.

2.3.2.3 RF rejection in FI

Connect the 0.1μF capacitor to the ground and introduce a 10 KHz signal into the general input of the circuit and verify the 10 KHz signal level in pin 12 of the LM1496. Determine the RF rejection level in IF.

How could we improve the rejection level in the different output signals ? Verify the circuit topology and the points by which the inputs connect to the output. Suggest possible mounting solutions or possible improvements in the quality of the components.

2.3.3 Measurements with the demodulator

Notice: Connect the capacitor between the Q1 transistor emitter and pin 7 of the LM1496 mixer. The supply voltage will be 15 V.

2.3.3.1 Evaluation of the demodulation and of the distorsion of the obtained signal

Once having mounted completely the circuit generate a AM modulated signal with a 10 KHz carrier frequency and a 1.3 KHz modulator frequency. Verify that the PLL output is a triangular 10 KHz signal and that the modulated signal is obtained at the output of the general circuit.

Take as reference signal the 1 KHz modulator for all following measurements. Measure the FFT level in dB of the signal with the oscilloscope before introducing it into the second generator (modulation).

About the demodulated signal:

- Measure its power level when compared to the reference signal.
- Measure the power level of the harmonics 2 and 3 of the demodulated signal (2 and 3 KHz) and the signal harmonics at 20 and 30 KHz.
- Is it possible to improve the final output signal by reducing the distortion in those harmonics? Analyze the signal that is being used for the coherent demodulation. How could it be improved?